IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#6/8 Bond 1/29/03

Applicant: Randolph

Serial No.: 10/032,646

Conf. No.: 5662

Filed: December 27, 2001

Title: PLANAR TRANSISTOR STRUCTURE USING ISOLATION IMPLANTS FOR IMPROVED VSS RESISTANCE AND FOR PROCESS SIMPLIFICATION

Art Group: 2811

Examiner: Loke, Steven Ho Yin

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate Under 37 C.F.R. § 1.8

I hereby certify this document is being deposited with sufficient postage, with the U.S. Postal Service as U.S. Express mail post office to Addressee service, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on or before the date indicated below:

Toni Stanley — TONI STANLEY — June 30, 2003

Signature — Printed Name — Date

RESPONSE TO OFFICE ACTION

In response to the Office Action mailed January 28, 2003 (Paper 4), with a three-month shortened statutory period for response set to expire on April 28, 2003, and hereby extended to June 30, 2003 by the attached Petition for Extension of Time, Applicant respectfully requests that